OIPE
JAN 0 2 2004
PATENT & TRADEMARK OFFICE
JC134

VERIFICATION OF TRANSLATION

I, Kenji FUJIMOTO

of a citizen of Japan residing at: 410, 14-1, Higashiyama-cho, Itabashi-ku, Tokyo 174-0073, Japan certify that I am familiar with the English and Japanese languages, and to the best of my knowledge and belief the following is a true translation of the officially certified copy of the Japanese Patent Application, 2000-354306

This 25 day of November, 2003

K. Fujimoto

Kenji FUJIMOTO

[Document Name] PATENT APPLICATION

[Identification No.] 01211282

[Filing Date] Heisei 12 November 21

[To] Commissioner of Japanese Patent Office

[International Patent Classification] H01L 21/82

[Inventor]

[Domicile or Residence] c/o NEC IC-Microcomputer System Corporation, 403-53, 1-chome, Kosugi-machi, Nakahara-ku, Kawasaki-city, Kanagawa prefecture, Japan

[Name] Hashimoto Eiki

[Applicant]

[ID number] 000232036

[Name] NEC IC-Microcomputer System Corporation

[Attorney]

[ID number] 100102864

[Patent Attorney]

[Name or Title] Minoru Kudoh

[Selected Attorney]

[ID number] 100099553

[Patent Attorney]

[Name or Title] Masao Ohomura

[Indication of Charge]

[Deposit Payment Register Number] 053213

[Amount of Fee] 21000yen

[Items of the Filing Articles]

[Article Name] Specification one copy

[Article Name] Drawings one copy

[Article Name] Abstract one copy

[General Power of Attorney] 9815548

5 [Proof] Necessary

[Document Name] Specification

[Title of the Invention] SEMICONDUCTOR CIRCUIT DESIGNING APPARATUS AND A SEMICONDUCTOR CIRCUIT DESIGNING METHOD

[Scope of Patent to be Claimed]

[Claim 1] A semiconductor circuit designing apparatus, comprising:

a circuit design unit executing a logical design of a semiconductor integrated circuit; and

an inspection item database section in which a circuit feature of said semiconductor integrated circuit corresponds to an inspection item of a acceptance inspection to be required before a layout design of said semiconductor integrated circuit,

wherein said circuit design unit generates a target circuit feature information indicating said circuit feature of a target semiconductor integrated circuit of said semiconductor integrated circuit, obtains a target inspection item of said inspection item corresponding to said target circuit feature information from said inspection item database section, and executes said logical design of said target semiconductor integrated circuit in reference to said target inspection item.

[Claim 2] The semiconductor circuit designing apparatus according to Claim 1, further comprising:

a model development history database in which

said circuit design unit corresponds to the number of times of failures of said inspection item, and

wherein said inspection item of which said number of times is small is withdrawn from said target inspection item.

[Claim 3] The semiconductor circuit designing apparatus according to Claim 1, further comprising:

a layout design unit executing said layout design, and

wherein said circuit design unit executes said acceptance inspection of said target semiconductor integrated circuit of which said layout design is executed, and provides a result of said acceptance inspection with said target semiconductor integrated circuit to said layout design unit.

[Claim 4] The semiconductor circuit designing apparatus according to Claim 1, wherein said inspection item database belongs to said circuit design unit.

[Claim 5] The semiconductor circuit designing apparatus according to Claim 3, wherein said inspection item database belongs to said layout design unit.

[Claim 6] The semiconductor circuit designing apparatus according to Claim 3, wherein said layout design unit includes a plurality of layout design sections, and

wherein said inspection item database section belongs to at least one of said plurality of layout design sections.

[Claim 7] The semiconductor circuit designing apparatus according to Claim 3, further comprising:

a data center provided to be different from said circuit design unit and said layout design unit, and

wherein said inspection item database belongs to said data center.

[Claim 8] A semiconductor circuit designing method, comprising:

generating a inspection item database in which a circuit feature of a semiconductor integrated circuit corresponds to an inspection item to be executed;

notifying a circuit designer of a target inspection item that is said inspection item corresponding to a target semiconductor integrated circuit for which said logical design is executed; and

executing said logical design of said target semiconductor integrated circuit in reference to said target inspection item.

[Claim 9] The semiconductor circuit designing method according to Claim 8, further comprising:

providing said target semiconductor integrated circuit in which said target inspection item is passed

to a layout designer.

[Claim 10] The semiconductor circuit designing method according to Claim 9, further comprising:

generating a model development history database in which said circuit designer corresponds to said inspection item and the number of times of failures of said inspection item, and

withdrawing said inspection item of which said number of times is small corresponding to said circuit designer from said target inspection item.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention belongs]

The present invention relates to a semiconductor circuit designing apparatus and a semiconductor circuit designing method. More particularly, the present invention relates to a semiconductor circuit designing apparatus and a semiconductor circuit designing method, which are used in a silicon interface field of an ASIC development so as to further reduce the number of steps in a circuit design and a layout design.

[0002]

[Conventional Technique]

In a field of a semiconductor design, a division between a circuit design and a layout design is advanced as a circuit becomes large and complex,

and the respective automations are advanced. In such division, an acceptance inspection is executed for examining whether or not a circuit information interfaced so as to minimize a backward motion of a step is reasonable. Inspection items for such an acceptance inspection are different depending on a circuit feature, such as a circuit configuration, a test simplifying method to be used and the like. So, the items of the acceptance inspection to be executed are determined depending on the circuit feature.

[0003]

A layout designer carries out all necessary acceptance inspections for each model, on the basis of the circuit information prepared by the circuit designer. So, a number of steps are needed in order to execute the acceptance inspection and confirm the result. Or, there may be a case that an acceptance inspection on the layout designer side is omitted by inquiring the executed inspection items of the circuit designer. However, an answer (entry) miss on the circuit designer side, a misunderstanding or the like causes an erroneous result to be reported, which results in the backward motion of the step (iteration) in many cases.

[0004]

A known drawing validation system disclosed in Japanese Laid Open Patent Application (JP-A-Heisei,

10-198708) includes a first memory for storing a data indicative of a drawing, a second memory for storing a data indicative of a predetermined condition and a judging unit for judging whether or not the drawing agrees with the predetermined condition. Such a drawing validation system can automatically validate whether or not an item specified on the basis of a know-how and an experience of the circuit designer is accurately reflected to thereby prepare a drawing of a layout of a printed circuit board, without any manual work. Thus, it is possible to prepare the drawing with high quality in a short time.

[0005]

This drawing validation system relates to a determination of an inspection item and an inspection execution in a single drawing validation system to be used by the layout designer. Its applicable department is limited to the layout designer side. Thus, it does not disclose a method to be used for the circuit designer to avoid a problem.

[0006]

[Problems the Invention Tries to Solve]

An object of the present invention is to provide a semiconductor circuit designing apparatus and a semiconductor circuit designing method, in which an iteration, such as a re-design and the like, caused by a design trouble can be reduced.

Another object of the present invention is to provide a semiconductor circuit designing apparatus and a semiconductor circuit designing method, in which inspection items can be reduced.

Still another object of the present invention is to provide a semiconductor circuit designing apparatus and a semiconductor circuit designing method, in which a burden of a number of steps on a circuit designer can be reduced.

Still another object of the present invention is to provide a semiconductor circuit designing apparatus and a semiconductor circuit designing method, in which a burden of a number of steps on a layout designer can be reduced.

[0007]

[Means for Solving the Problems]

The units to solve the object are described as follows. A number, a symbol and the like together with a parenthesis () are attached to a technical item appearing in the description. The number, the symbol and the like coincide with a reference number, a reference symbol and the like, which are given to the technical item constituting at least one implementation or a plurality of embodiments in a plurality of implementations or a plurality of embodiments in the present invention, especially, the technical item illustrated in a drawing corresponding

to the implementation or the embodiment. Those reference number and reference symbol clarify the correspondence and the relationship between the technical item noted in claim and the technical item in the implementation or the embodiment. Those correspondence and relationship do not imply that the technical item noted in claim is construed so as to be limited to the technical item in the implementation or the embodiment.

[0008]

A semiconductor circuit designing apparatus of the present invention, includes: a circuit design unit (1) executing a logical design of a semiconductor integrated circuit; and an inspection item database (6) section in which a circuit feature of the semiconductor integrated circuit corresponds to an inspection item of an acceptance inspection to be required before a layout design of the semiconductor integrated circuit, wherein the circuit design unit (1) generates a target circuit feature information indicating the circuit feature of a target semiconductor integrated circuit of the semiconductor integrated circuit, obtains a target inspection item of the inspection item corresponding to the target circuit feature information from the inspection item database (6) section, and executes the logical design of the target semiconductor integrated circuit in

reference to the target inspection item.

[0009]

The above-mentioned logical design enables the design data, in which the rejection in the acceptance inspection is smaller, to be provided to the layout designer.

[0010]

In this case, the semiconductor circuit designing apparatus further includes: a model development history database (7) in which the circuit design unit (1) corresponds to the number of times of failures of the inspection item, and wherein the inspection item of which the number of times is small is withdrawn from the target inspection item. Such an exemption reduces the number of the designing steps of the circuit designer.

[0011]

Also in this case, the semiconductor circuit designing apparatus further includes: a layout design unit (2) executing the layout design, and wherein the circuit design unit (1) executes the acceptance inspection of the target semiconductor integrated circuit of which the layout design is executed, and provides a result of the acceptance inspection with the target semiconductor integrated circuit to the layout design unit (2).

[0012]

Also in this case, the inspection item database (6) belongs to the circuit design unit (1). Or, the inspection item database (6) belongs to the layout design unit (2). Or, both of the circuit design unit (1) and the layout design unit (2) may include the inspection item database (6), respectively. The layout design unit includes a plurality of layout design sections, and wherein the inspection item database (6) belongs to at least one of the plurality of layout design sections. Here, at least one does not imply all of the plurality of units, and it implies one or the plurality of layout designing units.

[0013]

Also in this case, the semiconductor circuit designing apparatus further includes: a data center provided to be different from the circuit design unit (1) and the layout design unit (2), and wherein the inspection item database (6) belongs to the data center. The inspection item database (6) is unitarily managed by the data center unit and easily updated.

[0014]

A semiconductor circuit designing method of the present invention, includes: generating a inspection item database (6) in which a circuit feature of a semiconductor integrated circuit corresponds to an inspection item to be executed; notifying a circuit designer of a target inspection item that is the

inspection item corresponding to a target semiconductor integrated circuit for which the logical design is executed; and executing the logical design of the target semiconductor integrated circuit in reference to the target inspection item. The above-mentioned logical design enables the design data, in which the rejection in the acceptance inspection is smaller, to be provided to the layout designer.

[0015]

In this case, the semiconductor circuit designing method, further includes: providing the target semiconductor integrated circuit in which the target inspection item is passed to a layout designer. According to such a provision, the frequency at which the layout designer requests the re-logical design of the target semiconductor integrated circuit is reduced.

[0016]

In this case, the semiconductor circuit designing method further includes: generating a model development history database (7) in which the circuit designer corresponds to the inspection item and the number of times of failures of the inspection item, and withdrawing the inspection item of which the number of times is small corresponding to the circuit designer from the target inspection item. Such an exemption reduces the number of the designing steps of the circuit designer.

[0017]

[Embodiments of the Invention]

With reference to the attached drawings, an embodiment of a semiconductor designing system according to the present invention, a plurality of engineering workstations (hereafter, abbreviated as [EWS]) are connected to each other. The plurality of EWS are provided with a circuit design EWS1 and a layout design EWS2. They are connected to each other through a network 3.

[0018]

The circuit design EWS1 is installed for each circuit designer and used for a circuit design. For example, the circuit design EWS1 belongs to a circuit designer A, and a circuit design EWS1' belongs to a circuit designer B. Circuit designers ID different from each other are assigned to the circuit designers. The circuit designer ID is used to identify the circuit designer and identify a right under which the circuit designer accesses the layout design EWS2. The circuit designer is one person or a plurality of persons attached to one group. That group is an enterprise, a department within an enterprise, a design group within a department or the like. The circuit design EWS1 has a check sheet 4. The check sheet 4 is an interface file in which a circuit feature of a semiconductor integrated circuit, an

inspection item and an inspection result are noted. The check sheet 4 is prepared for each circuit design.

[0019]

The layout design EWS2 belongs to a layout designer, and it is used for the layout design. The layout designer gives the circuit designer ID to each circuit designer. The layout design EWS2 has an inspection item database 6 and a model development history database 7. The inspection item database 6 is noted while a circuit feature and an inspection item necessary for the circuit feature are correlated to each other. The model development history database 7 is noted while a circuit designer ID of a designing circuit designer, a circuit feature of a previously designed semiconductor integrated circuit and a frequency of errors occurring in the development step are correlated to each other.

[0020]

Fig. 2 shows an actual example of the check sheet 4. The circuit feature, the inspection item and an inspection result are noted in the check sheet 4. A technology, a condition, a model name, a package, a number of pins, a presence or absence of a usage of a test simplifying method are noted as the circuit feature. The test simplifying method uses a scan, a boundary scan and RAM. A net list check, a pattern check, a scan check, a timing check and the like are

noted as the inspection items.

[0021]

In the semiconductor integrated circuit according to this embodiment on which the acceptance inspection is performed, the technology is CMOS9HD, the condition is 3.3 V, the model name is 65956E00, the package is TBG, and the number of pins is 420 pins. Moreover, the scan manner of the test simplifying method is used without using the boundary scan and the RAM. The inspection items necessary for this semiconductor integrated circuit are the net list check, the pattern check, the scan check and the timing check. As the inspection result, there is no error in the net list check, there are two errors in the pattern check, the scan check is not executed, and there is no error in the timing check.

[0022]

Fig. 3 shows an actual example of the inspection item database 6. As for the semiconductor integrated circuit, the inspection items are different depending on the circuit feature. The inspection items necessary for the respective circuit features of the semiconductor integrated circuit are noted in the inspection item database 6. As the circuit feature, there are a basic configuration, a usage of the scan, a usage of the boundary scan, a usage of the RAM, a test bus configuration and the like. As the

inspection items, there are the net list check, the pattern check, the scan check, the boundary scan check, the timing check, a test terminal check and a RAM check.

[0023]

If the semiconductor integrated circuit on which the acceptance inspection is performed is designed by only the basic configuration, the inspection items in the acceptance inspection that must be executed are the net list check, the pattern check and the timing check. If the semiconductor integrated circuit on which the acceptance inspection is performed employs the scan manner that is the test simplifying method, the inspection items in the acceptance inspection that must be executed are the net list check, the pattern check, the scan check and the timing check.

[0024]

If the semiconductor integrated circuit on which the acceptance inspection is performed employs the boundary scan manner that is the test simplifying method, the inspection items in the acceptance inspection that must be executed are the net list check, the pattern check, the boundary scan check and the timing check. If the semiconductor integrated circuit on which the acceptance inspection is performed employs the RAM, they are the net list check,

the pattern check, the timing check and the RAM check. If the semiconductor integrated circuit on which the acceptance inspection is performed has the test bus configuration, the inspection items in the acceptance inspection that must be executed are the net list check, the pattern check, the timing check and the test terminal check.

[0025]

Such an inspection item database 6 clarifies the inspection items in the acceptance inspection to be executed. This results in the sure execution of the acceptance inspection.

[0026]

Fig. 4 shows an actual example of the model development history database 7. In the model development history database 7, the designer ID, the circuit feature and the inspection result are noted while they are correlated to each other, for each semiconductor integrated circuit.

[0027]

For example, in a case of a semiconductor integrated circuit having a model name of 6595E00 that is designed by a circuit designer whose circuit designer ID is AAA, its technology is COMS9HD, its condition is COMS3,3V, and its package is TBG. As the various inspection results of this semiconductor integrated circuit, there is no error in the net list

check, there are two errors in the pattern check, the scan check is not executed, and there is no error in the timing check, in the acceptance inspection executed on September 11.

[0028]

In a re-acceptance inspection executed on September 14, there is no error in the net list check, there is no error in the pattern check, the scan check is not executed, and there is no error in the timing check. In a back annotation executed on September 18, there is no error in the net list check, there are two errors in the pattern check, there is no error in the scan check, and there is no error in the timing check.

[0029]

Figs. 5, 6 show the operation of the semiconductor designing system according to the present invention. At first, a circuit designer inputs a circuit designer ID to the circuit design EWS1 (Step S1). The circuit design EWS1 sends the input circuit designer ID through the network 3 to the layout design EWS2.

[0030]

The layout design EWS2 judges an allowance or rejection of an access in accordance with the circuit designer ID (Step S2). If it is judged that there is no problem in the circuit designer ID, the access is allowed, and the layout design EWS2 reports its fact

to the circuit design EWS1. If the access is allowed, the circuit designer inputs to the circuit design EWS1 the circuit feature of a semiconductor integrated circuit to be designed. The circuit design EWS1 sends the circuit feature to the layout design EWS2 (Step S3).

[0031]

The layout design EWS2 obtains the circuit designer ID and the circuit feature, retrieves an inspection item to be inspected on the basis of the inspection item database 6, and retrieves a previous error of the circuit designer designing the semiconductor integrated circuit on the basis of the model development history database 7 (Step S4). The layout design EWS2 determines an inspection item to be executed at this time on the basis of the retrieved inspection item and error (Step S5).

[0032]

For example, if there is an inspection item having no problem in five models finally developed by the circuit designer, an execution of the inspection item is exempted. If there is an item in which an error is recorded in the model development history database, the item is determined to be an inspection item to be executed. Such exemption enables the number of inspection items to be reduced on the basis of the experience and the level of the circuit

designer. Thus, the burden on the circuit designer is relaxed. If the circuit designer is composed of a plurality of designers, the exempted inspection items are greater to further relax the burden on the circuit designer.

[0033]

The layout design EWS2 sends the determined execution inspection item to the circuit design EWS1. The circuit design EWS1 receives the execution inspection item from the layout design EWS2, and writes the inspection items and the circuit feature of the semiconductor integrated circuit to the check sheet 4 (Step S6). The circuit design EWS1 displays a previous error content received from the layout design EWS2 on a screen. The circuit designer designs a logical circuit while paying attention to the previous error content and the execution inspection item (Step S7). Since the item to which the attention must be paid can be obtained at an initial stage of a logical design, the circuit designer can avoid a logical design unsuitable for a layout design and accordingly avoid the re-design (iteration).

[0034]

If the design of the logical circuit is completed, a logical validation of the logical design is executed (Step S8). If any trouble is discovered in the logical validation, the logical design is again

carried out. After the completion of the logical design, the circuit design EWS1 checks the acceptance inspection item noted in the check sheet 4 (Step S9). The inspection result is additionally written to the check sheet 4. If there is a rejected item among the inspection items noted in the check sheet 4, the logical design is again carried out. Such re-design can prevent an unnecessary iteration in advance. If there is no problem in all the items among the acceptance inspection items, the circuit design EWS1 sends the check sheet 4 together with the design data such as a circuit connection information, a pattern and the like to the layout design EWS2 (Step S10).

[0035]

The layout design EWS2 compares the execution inspection items noted in the check sheet 4 with the executed result, in response to the reception of the check sheet 4. If there is an inspection item in which the executed result is not noted in the inspection items to be executed, it is judged as a non-execution, and it is returned back to the circuit designer, and the inspection of the non-execution item is requested (Step S11). If there is a result unsuitable for the layout as the result of the acceptance inspection, it is returned back to the circuit designer, and the improvement based on the re-design is requested (Step S12). If the layout has no

problem in all the inspection items, the inspection result together with the circuit feature and the circuit designer ID is written to the model development history database 7.

[0036]

After that, the layout designer designs the layout (Step S13). After the design of the layout, a back annotation is carried out (Step S14). In the back annotation, it is confirmed whether or not the semiconductor integrated circuit carries out a desirably functional operation at a delay after the layout, and additionally writes its result to the model development history database 7. If the result of the back annotation is NG, it is returned back to the circuit designer, and the improvement based on the re-design is requested. If the result of the back annotation is OK, an EB process is carried out (Step S15).

[0037]

Incidentally, the back annotation may be executed by the circuit designer. At this time, after the design of the layout, the layout design data is sent from the layout design EWS2 to the circuit design EWS1, and the circuit design EWS1 executes the back annotation. If the back annotation is NG, the logical design is again carried out. If the back annotation is OK, the circuit design EWS1 sends its fact to the

layout design EWS2. The layout designer carries out the EB process, in response to the report of the back annotation OK.

[0038]

By correlating between the previous error and problem and the circuit feature and the circuit designer, the circuit designer can obtain the items to be considered at the time of the logical design prior to the designing and thereby avoid the problem at the stage of the logical design. Also, since the circuit designer executes the acceptance inspection, the acceptance inspection of the layout designer is not required, which reduces the number of steps in the layout designer. Moreover, it is possible to reduce the request of the re-design to the circuit designer from the layout designer side caused by the defective result of the acceptance inspection. Such dispersion of the process can attain a further reduction in TAT.

[0039]

Figs. 7, 8 show another operation of the semiconductor designing system according to the present invention. At first, a circuit designer inputs a circuit designer ID to the circuit design EWS1 (Step S21). The circuit design EWS1 sends the input circuit designer ID through the network 3 to the layout design EWS2.

[0040]

The layout design EWS2 judges an allowance or rejection of an access in accordance with the circuit designer ID (Step S22). If it is judged that there is no problem in the circuit designer ID, the access is allowed, and the layout EWS2 reports its fact to the circuit design EWS1. If the access is allowed, the circuit designer inputs to the circuit design EWS1 the circuit feature of a semiconductor integrated circuit to be designed (Step S23). The circuit design EWS1 sends the circuit feature to the layout design EWS2.

[0041]

The layout design EWS2 obtains the circuit designer ID and the circuit feature, and retrieves an inspection item to be inspected on the basis of the inspection item database 6, and then retrieves a previous error of the circuit designer designing the semiconductor integrated circuit on the basis of the model development history database 7 (Step S24). The layout design EWS2 determines an inspection item to be executed at this time on the basis of the retrieved inspection item and error (Step S5). For example, if there is an inspection item having no problem in five models finally developed by the circuit designer, an execution of the inspection item is exempted. If there is an item in which an error is recorded in the model development history database, the item is determined to be an inspection item to be executed.

The layout design EWS2 sends the determined inspection item to the circuit design EWS1.

[0042]

The circuit design EWS1 receives the execution inspection item from the layout design EWS2, and writes the inspection items and the circuit feature of the semiconductor integrated circuit to the check sheet 4 (Step S26). The circuit design EWS1 displays a previous error content received from the layout design EWS2 on the screen. The circuit designer designs a logical circuit while paying attention to the previous error content (Step S27). If the design of the logical circuit is completed, a logical validation of the logical design is executed (Step S28). If any trouble is discovered in the logical validation, the logical design is again carried out.

[0043]

After the completion of the logical design, the circuit design EWS1 checks the acceptance inspection item noted in the check sheet 4 (Step S29). The inspection result is additionally written to the check sheet 4. If there is a rejected item among the inspection items noted in the check sheet 4, the logical design is again carried out. If there is no problem in all the items among the acceptance inspection items, the circuit design EWS1 sends the check sheet 4 together with the design data such as a

circuit connection information, a pattern and the like to the layout design EWS2 (Step S30).

[0044]

The layout design EWS2 compares the execution inspection items noted in the check sheet 4 with the executed result, in response to the reception of the check sheet 4 (Step S31). If there is an inspection item in which the executed result is not noted in the inspection items to be executed, it is judged as a non-execution, and its inspection item is inspected (Step S32). If there is a result unsuitable for the layout as the result of the acceptance inspection, it is returned back to the circuit designer, and the improvement based on the re-design is requested (Step S33). If the layout has no problem in all the inspection items, the inspection result together with the circuit feature and the circuit designer ID is written to the model development history database 7.

[0045]

After that, the layout designer designs the layout (Step S34). After the design of the layout, the back annotation is carried out (Step S35). The layout design EWS2 additionally writes the result of the back annotation to the model development history database 7. If the result of the back annotation is NG, it is returned back to the circuit designer, and the improvement based on the re-design is requested.

Incidentally, the back annotation may be executed by the circuit designer, similarly to the above-mentioned embodiment. If the result of the back annotation is OK, the EB process is carried out (Step S36).

[0046]

Since the inspection result of the acceptance inspection executed by the circuit designer is written to the check sheet 4, it is not necessary that the same inspection item is again executed in an acceptance inspection on a layout designer side. This results in the reduction of the number of the inspection steps of the layout designer. Moreover, since the number of steps in the acceptance inspection can be reduced, the circuit designer can be devoted entirely to the logical design.

[0047]

Figs. 9, 10 show the operation of the semiconductor designing system according to the present invention. At first, a circuit designer inputs a circuit designer ID to the circuit design EWS1 (Step S61). The circuit design EWS1 sends the input circuit designer ID through the network 3 to the layout design EWS2.

[0048]

The layout design EWS2 judges an allowance or rejection of an access in accordance with the circuit designer ID (Step S62). If it is judged that there is

no problem in the circuit designer ID, the access is allowed, and the layout EWS2 reports its fact to the circuit design EWS1. If the access is allowed, the circuit designer inputs to the circuit design EWS1 the circuit feature of a semiconductor integrated circuit to be designed. The circuit design EWS1 sends the circuit feature to the layout design EWS2 (Step S63).

[0049]

The layout design EWS2 obtains the circuit designer ID and the circuit feature, and retrieves an inspection item to be inspected on the basis of the inspection item database 6, and then retrieves a previous error of the circuit designer designing the semiconductor integrated circuit on the basis of the model development history database 7 (Step S64). The layout design EWS2 determines an inspection item to be executed at this time on the basis of the retrieved inspection item and error (Step S65). For example, if there is an inspection item having no problem in five models finally developed by the circuit designer, an execution of the inspection item is exempted. If there is an item in which an error is recorded in the model development history database, the item is determined to be an inspection item to be executed. The layout design EWS2 sends the determined inspection item to the circuit design EWS1.

[0050]

The circuit design EWS1 receives the execution inspection item from the layout design EWS2, and writes the inspection items and the circuit feature of the semiconductor integrated circuit to the check sheet 4 (Step S66). The circuit design EWS1 displays a previous error content received from the layout design EWS2 on the screen. The circuit designer designs a logical circuit while paying attention to the previous error content (Step S67). If the design of the logical circuit is completed, a logical validation of the logical design is executed (Step S68). If any trouble is discovered in the logical validation, the logical design is again carried out.

[0051]

The circuit design EWS1 examines whether or not an item equivalent to the inspection item of the acceptance inspection to be executed is included in the inspection items in the logical validation. If it is included, the inspection result of that item is written to the check sheet 4 (Step S69). Such representation can protect the same inspection from being doubly executed, which can reduce the number of steps in the circuit designer. After that, the circuit design EWS1 checks the acceptance inspection items noted in the check sheet 4 (Step S70), and additionally writes the inspection result to the check sheet 4.

[0052]

If there is a rejected item among the inspection items noted in the check sheet 4, the logical design is again carried out. If there is no problem in all the items among the acceptance inspection items, the circuit design EWS1 sends the check sheet 4 together with the design data such as the circuit connection information, the pattern and the like to the layout design EWS2 (Step S71).

[0053]

The layout design EWS2 compares the execution inspection items noted in the check sheet 4 with the executed result, in response to the reception of the check sheet 4. If there is an inspection item in which the executed result is not noted in the inspection items to be executed, it is judged as a non-execution, and it is returned back to the circuit designer, and the inspection of the non-execution item is requested (Step S72). If there is a result unsuitable for the layout as the inspection result of the acceptance inspection, it is returned back to the circuit designer, and the improvement based on the re-design is requested (Step S73). If the layout has no problem in all the inspection items, the inspection result together with the circuit feature and the circuit designer ID is written to the model development history database 7.

[0054]

After that, the layout designer designs the layout (Step S74). After the design of the layout, the back annotation is carried out (Step S75). In the back annotation, it is confirmed whether or not the semiconductor integrated circuit carries out a desirably functional operation at a delay after the layout, and additionally writes its result to the model development history database 7. If the result of the back annotation is NG, it is returned back to the circuit designer, and the improvement based on the re-design is requested. If the result of the back annotation is OK, the EB process is carried out (Step S76).

[0055]

Fig. 11 shows another embodiment of the semiconductor designing system according to the present invention. A circuit design EWS1 has a check sheet 4 and an inspection item database 6. A layout design EWS2 has a model development history database 7. At this time, the check sheet 4 is different from the previous embodiment. A circuit feature and an inspection result are written thereto, or only an inspection item to be executed and its inspection result are written thereto.

[0056]

Figs. 12, 13 show the operation of the

semiconductor designing system according to another embodiment of the present invention. At first, the circuit designer inputs to the circuit design EWS1 the circuit feature of the semiconductor integrated circuit to be designed (Step S41). The circuit design EWS1 retrieves an error when previously designing the semiconductor integrated circuit, on the basis of the model development history database 7 (Step S42). The circuit design EWS1 determines an inspection item to be executed at this time, in accordance with the retrieved inspection item (Step S43).

[0057]

The circuit design EWS1 writes to the check sheet 4 the circuit feature of the semiconductor integrated circuit and the inspection item to be executed (Step S44), and displays the previous error content on the screen. The circuit designer designs the logical circuit while paying attention to the previous error content (Step S45). If the design of the logical circuit is completed, a logical validation of the logical circuit is carried out (Step S46). If any trouble is discovered in the logical validation, the logical design is again carried out.

[0058]

After the completion of the logical design, the circuit design EWS1 checks the acceptance inspection item noted in the check sheet 4 (Step S47). The

inspection result is additionally written to the check sheet 4. If there is a rejected item among the inspection items noted in the check sheet 4, the logical design is again carried out. If there is no problem in all the items among the acceptance inspection items, the circuit designer inputs a circuit designer ID to the circuit design EWS1 (Step S48). The circuit design EWS1 sends the input circuit designer ID through the network 3 to the layout design EWS2.

[0059]

The layout design EWS2 judges an allowance or rejection of an access in accordance with the circuit designer ID (Step S49). If it is judged that there is no problem in the circuit designer ID, the access is allowed, and the layout EWS2 reports its fact to the circuit design EWS1. In the circuit designer, if the access is allowed, the circuit design EWS1 sends to the circuit design EWS2 the check sheet 4 together with the design data, such as the circuit connection information, the pattern and the like (Step S50).

[0060]

The layout design EWS2 compares the execution inspection items noted in the check sheet 4 with the executed result, in response to the reception of the check sheet 4 (Step S51). If there is an inspection item in which the executed result is not noted in the

inspection items to be executed, it is judged as a non-execution, and it is returned back to the circuit designer, and the inspection of the non-execution item is requested. If there is a result unsuitable for the layout as the result of the acceptance inspection, it is returned back to the circuit designer, and the improvement based on the re-design is requested (Step S52). If the layout has no problem in all the inspection items, the inspection result together with the circuit feature and the circuit designer ID is written to the model development history database 7.

[0061]

After that, the layout designer designs the layout (Step S53). After the design of the layout, the back annotation is carried out (Step S54). In the back annotation, it is confirmed whether or not the semiconductor integrated circuit carries out a desirably functional operation at a delay after the layout, and additionally writes its result to the model development history database 7. If the result of the back annotation is NG, it is returned back to the circuit designer, and the improvement based on the re-design is requested. If the result of the back annotation is OK, the EB process is carried out (Step S55).

[0062]

Such a semiconductor circuit designing system

can clarify the inspection item to be executed without any intervention of the network 3 by the circuit design EWS1. In the logical design in which the previous error is not displayed and the inspection item is not exempted, a communication between the circuit design EWS1 and the layout design EWS2 is small and efficient. Incidentally, the inspection item database may be simultaneously installed in both the circuit design EWS1 and the layout design EWS2. In this case, the semiconductor circuit designing system is operated as shown in Figs. 12, 13, similarly to this embodiment.

[0063]

Still another embodiment of the semiconductor designing system according to the present invention includes a plurality of layout designs EWS. As shown in Fig. 14, a layout design EWS2 belongs to a layout designer A, and a layout design EWS2' belongs to a layout designer B. The semiconductor designing system according to still another embodiment of the present invention further includes a data center 8. The data center 8 is connected to the network 3, and it has a inspection item database 6 and a model development history database 7.

[0064]

The circuit EWS1 obtains the data of the inspection item database 6 through the network 3 from

the data center 8. The layout EWS2 obtains the data of the inspection item database 6 or the model development history database 7 through the network 3 from the data center 8. The layout EWS2 further updates the data of the model development history database 7 through the network 3.

[0065]

If each of the plurality of layouts EWS has the inspection item database 6 and the model development history database 7, the database is managed by each layout EWS2, and the database is updated by each layout EWS2. In the semiconductor designing system according to still another embodiment of the present invention, the inspection item database 6 or the model development history database 7 is unitarily managed. It is easy to update the inspection item database 6 or the model development history database 7.

[0066]

Incidentally, a layout EWS2 that is a part of the plurality of layouts EWS2 may also hold the function of the data center without separately installing the data center 8.

[0067]

[Effects of the invention]

The semiconductor circuit designing apparatus and the semiconductor circuit designing method according to the present invention can avoid the

occurrence of the problem in the later step in advance by providing the inspection items in the acceptance inspection to the circuit designer.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a block diagram showing a configuration of a semiconductor design system according to a embodiment of the present invention;

[Fig. 2]

Fig. 2 is a table of a check sheet of a semiconductor design system according to a embodiment of the present invention;

[Fig. 3]

Fig. 3 is a table of a inspection item database of a semiconductor design system according to a embodiment of the present invention;

[Fig. 4]

Fig. 4 is a table of a model development history database of a semiconductor design system according to a embodiment of the present invention;

[Fig. 5]

Fig. 5 is a flow chart of semiconductor design method according to a embodiment of the present invention;

[Fig. 6]

Fig. 6 is a flow chart of semiconductor design method according to a embodiment of the present

invention;

[Fig. 7]

Fig. 7 is a flow chart of semiconductor design method according to another embodiment of the present invention;

[Fig. 8]

Fig. 8 is a flow chart of semiconductor design method according to another embodiment of the present invention;

[Fig. 9]

Fig. 9 is a flow chart of semiconductor design method according to still another embodiment of the present invention;

[Fig. 10]

Fig. 10 is a flow chart of semiconductor design method according to still another embodiment of the present invention;

[Fig. 11]

Fig. 11 is a block diagram showing a configuration of a semiconductor design system according to another embodiment of the present invention;

[Fig. 12]

Fig. 12 is a flow chart of semiconductor design method according to yet still another embodiment of the present invention;

[Fig. 13]

Fig. 13 is a flow chart of semiconductor design method according to yet still another embodiment of the present invention; and

[Fig. 14]

Fig. 14 is a block diagram showing a configuration of a semiconductor design system according to still another embodiment of the present invention.

[Description of the reference Numerals and Symbols]

1 circuit design EWS

2 layout design EWS

3 network

4 check sheet

6 inspection item database 6

7 model development history database

8 data center

[Document Name] Abstract

[Abstract]

[Object] An iteration, such as a re-design and the like, caused by a design trouble is reduced and a burden of a number of steps on a circuit designer is reduced.

[Solving Means]

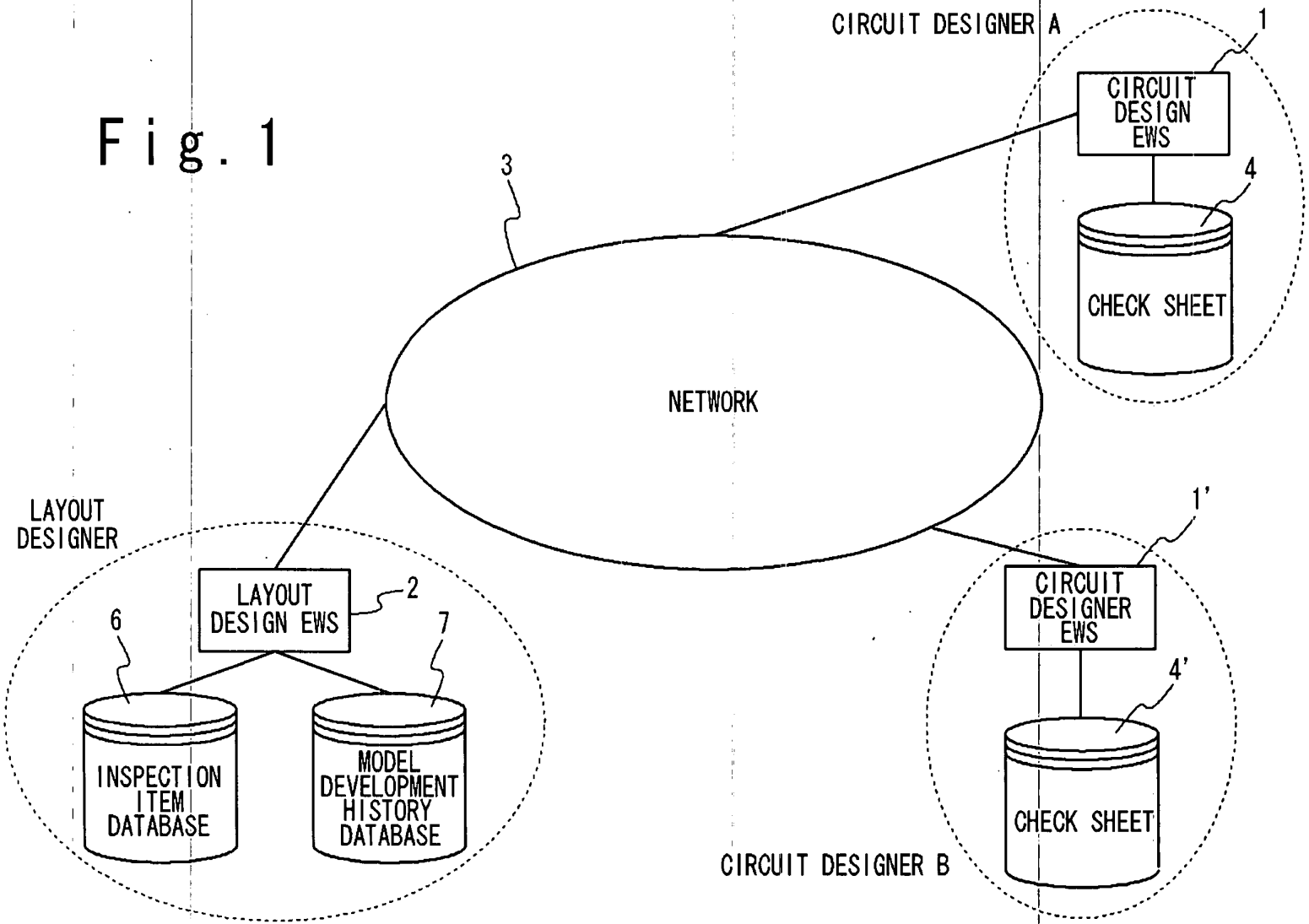
A semiconductor circuit designing apparatus includes an inspection item database 6 which corresponds to an inspection item of a acceptance inspection and a circuit design unit 1, wherein the

circuit design unit 1 obtains a target inspection item corresponding to a circuit feature of a target circuit, and executes a logical design of a target semiconductor integrated circuit based on the target inspection item. A model development history database in which the circuit design unit 1 corresponds to the number of times of failures of the inspection item is further included and the inspection item of which the number of times is small is withdrawn from the target inspection item. A layout design unit 2 is further included and the circuit design unit 1 executes the acceptance inspection of the target semiconductor integrated circuit of which the layout design is executed, and provides a result of the acceptance inspection with the target semiconductor integrated circuit to the layout design unit 2.

[Selected Drawing] Fig.1

OIPE
JAN 0 2 2004
PATENT & TRADEMARK OFFICE
JC13

Fig. 1



PATENT & TRADEMARK OFFICE
JAN 02 2004

Fig. 2

4:CHECK SHEET

CIRCUIT FEATURE								INSPECTION ITEM AND RESULT			
TECHNOLOGY	CONDITION	MODEL NAME	PACKAGE	THE NUMBER OF PINS	SCAN	BOUNDARY SCAN	RAM	NET LIST CHECK	PATTERN CHECK	SCAN CHECK	TIMING CHECK
CMOS9HD	cmos_3.3V	65956E00	TBG	420	USED	NOT-USED	NOT-USED	ERROR 0	ERROR 2	NOT-EXECUTED	ERROR 0

PATENT & TRADEMARK OFFICE JAN 0 2 2004 OIPE

Fig. 3

6: INSPECTION ITEM DATABASE

CIRCUIT FEATURE	INSPECTION ITEM						
	NET LIST CHECK	PATTERN CHECK	SCAN CHECK	BOUNDARY SCAN CHECK	TIMING CHECK	TEST TERMINAL CHECK	RAM CHECK
BASIC CONFIGURATION	EXECUTED	EXECUTED			EXECUTED		
USAGE OF THE SCAN	EXECUTED	EXECUTED	EXECUTED		EXECUTED		
USAGE OF THE BOUNDARY SCAN	EXECUTED	EXECUTED		EXECUTED	EXECUTED		
USAGE OF THE RAM	EXECUTED	EXECUTED			EXECUTED		EXECUTED
TEST BUS CONFIGURATION	EXECUTED	EXECUTED			EXECUTED	EXECUTED	
...	...	...	...	...	...	...	...

OIPE
PATENT & TRADEMARK OFFICE
JAN 0 2 2004
JC194

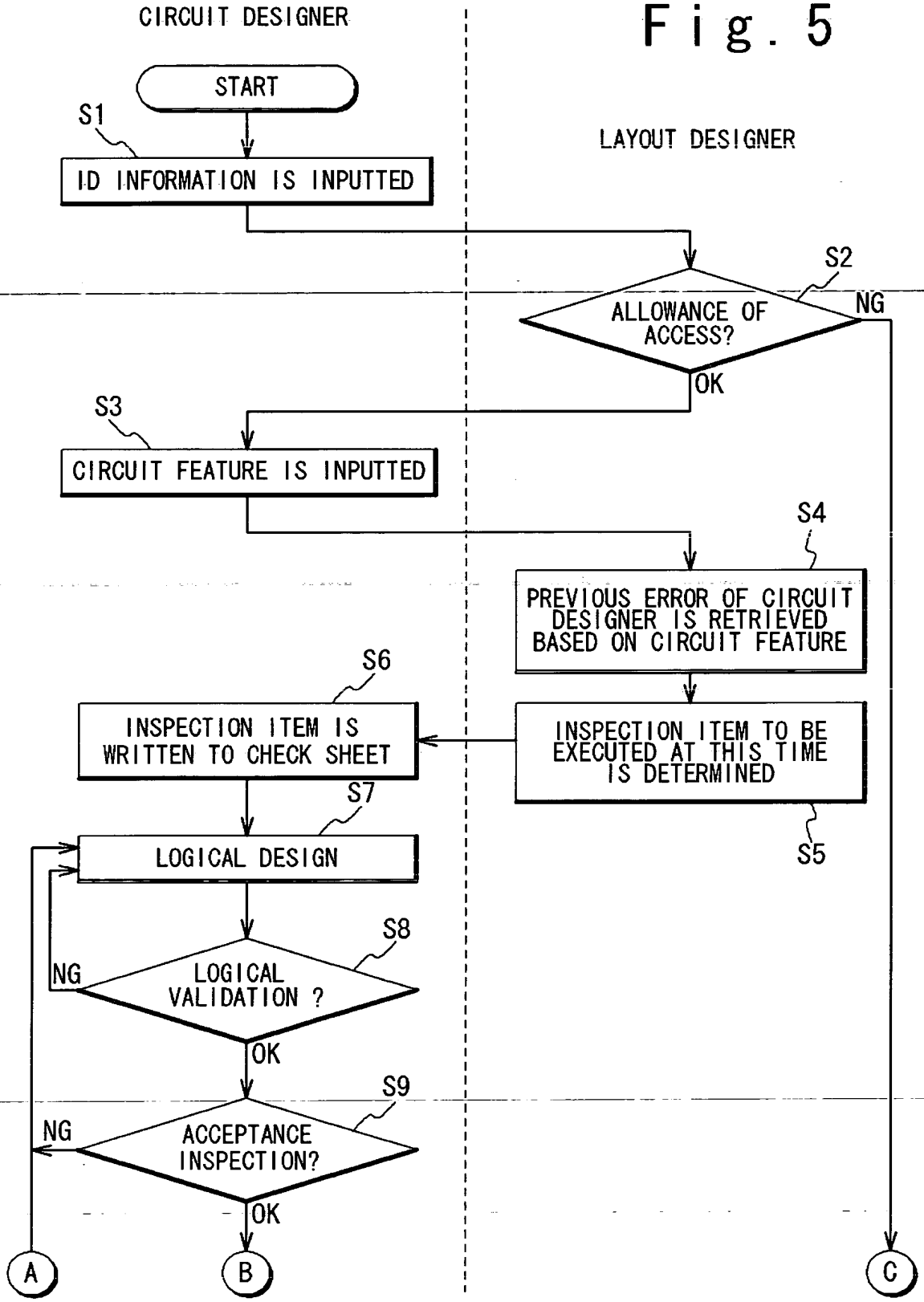
Fig. 4

7:MODEL DEVELOPMENT HISTORY DATABASE

IDINFORMATION	CIRCUIT FEATURE					INSPECTION ITEM ECXECUTION HISTORY							
	TECHNOLOGY	CONDITION	MODEL NAME	PACKAGE	:	PHASE	DATA	NET LIST CHECK	PATTERN CHECK	SCAN CHECK	BOUNDARY SCANCHECK	TIMING CHECK	:
AAA	CMOS9HD	cmos_3.3V	6595 6E00	TBG	:	ACCEPTED	9/11	ERROR 0	ERROR 2	NOT-EXECUTED	NOT-TARGETED	ERROR 0	:
						RE-ACCEPTED	9/14	ERROR 0	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	:
						BACK ANNOTATION	9/18	ERROR 0	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	:
	CB7	ttl_5V	87543	QOGN	:	ACCEPTED	9/4	EXCEPTED	ERROR 0	NOT-TARGETED	ERROR 0	ERROR 0	:
						BACK ANNOTATION	9/11	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	ERROR 0	:
ABC	CB8	ttl_3.3V	12345	A8SI	:	ACCEPTED	8/3	ERROR 0	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	:
						BACK ANNOTATION	8/7	ERROR 0	ERROR 0	ERROR 0	NOT-TARGETED	ERROR 0	:
	CMOS6	cmos_5V	6562 4E99	QFP	:	ACCEPTED	7/29	ERROR 0	ERROR 0	NOT-TARGETED	NOT-TARGETED	ERROR 0	:
						BACK ANNOTATION	9/4	ERROR 0	ERROR 0	NOT-TARGETED	NOT-TARGETED	ERROR 0	:
	:	:	:	:		:	:	:	:	:	:	:	

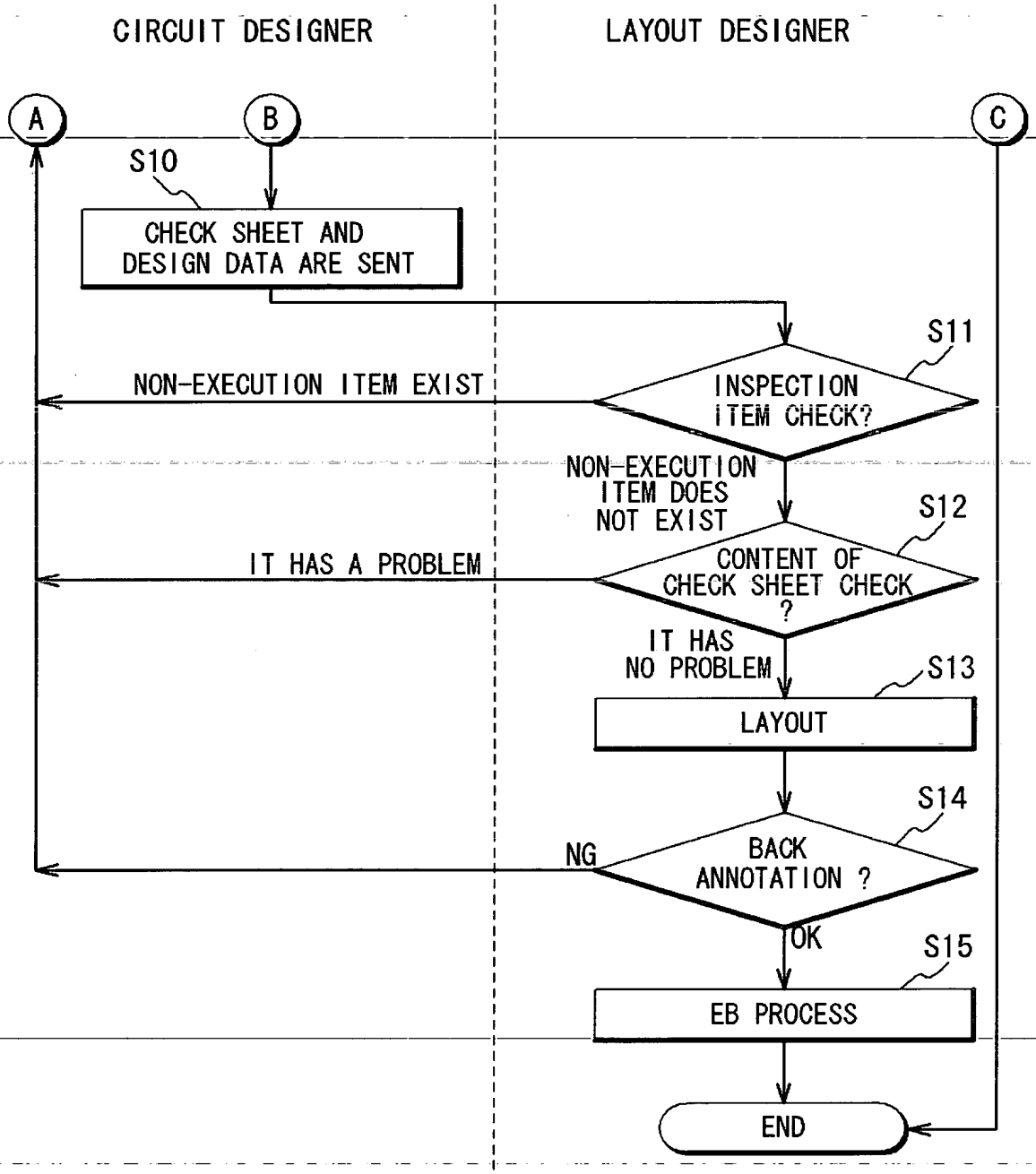
OIPE JC184
JAN 0 2 2004
PATENT & TRADEMARK OFFICE

Fig. 5



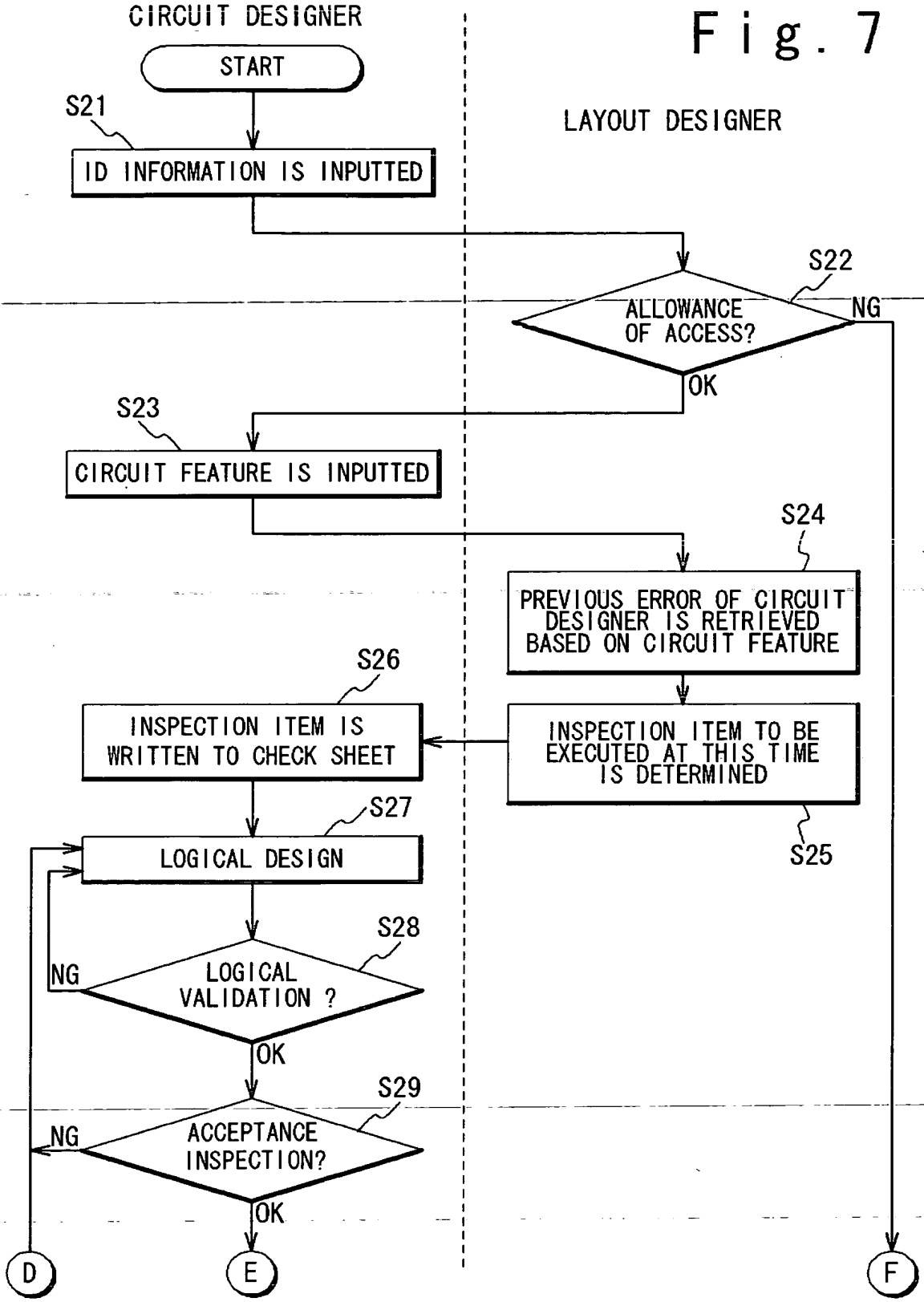
OIPE JC134
JAN 0 2 2004
PATENT & TRADEMARK OFFICE

Fig. 6



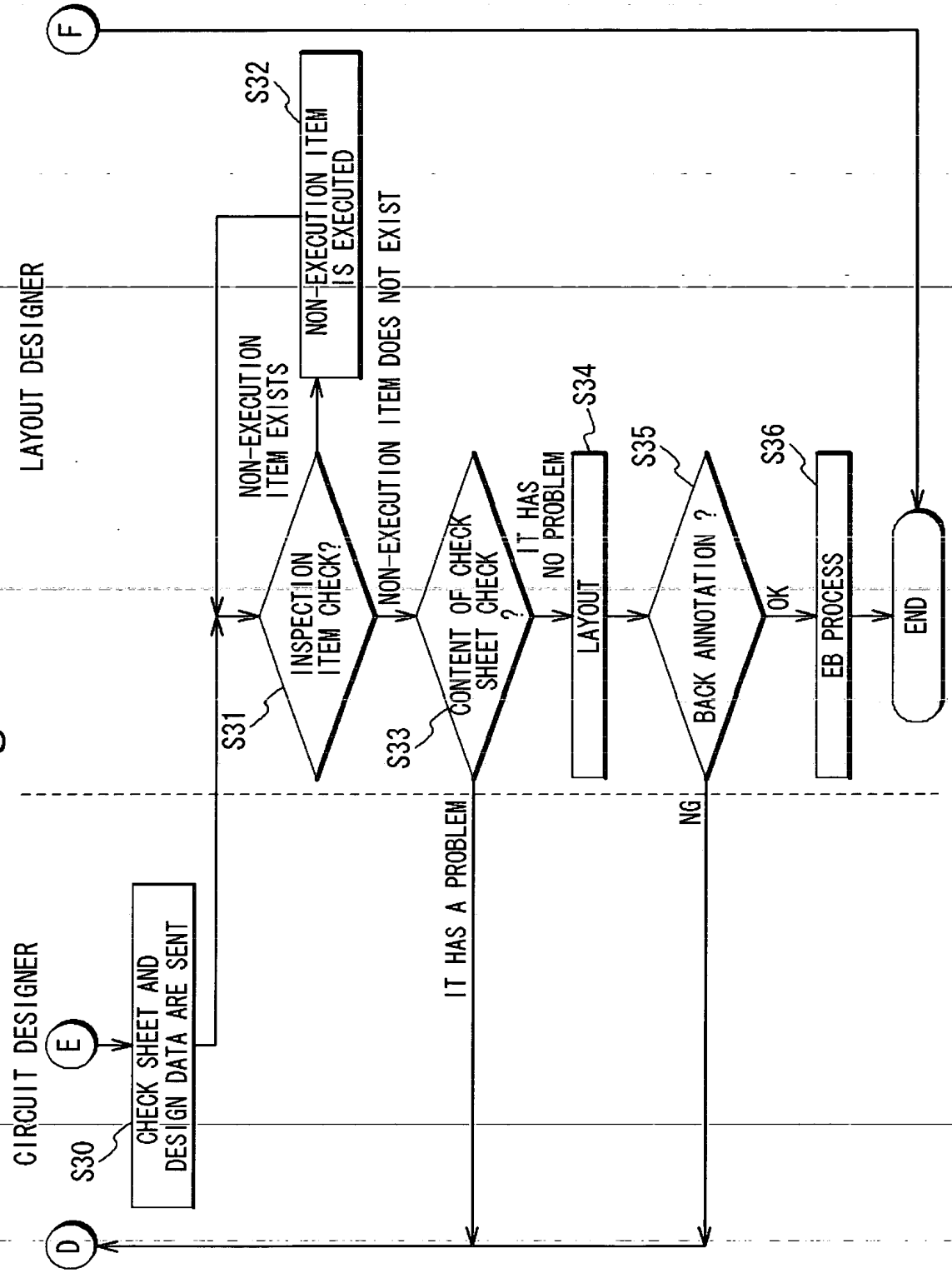
OIPE JC194
JAN 0 2 2004
PATENT & TRADEMARK OFFICE

Fig. 7



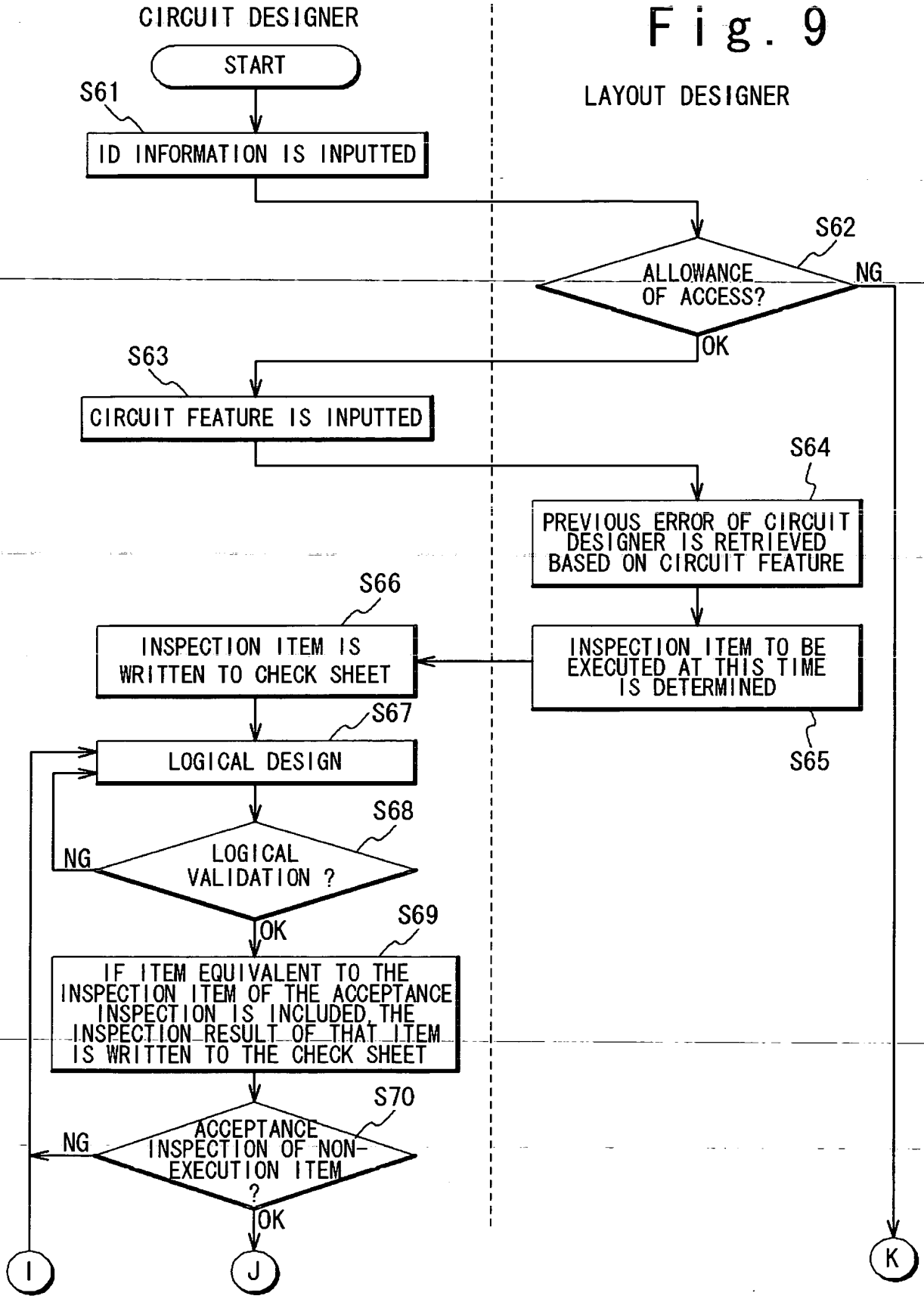
OIPE JC184
JAN 0 2 2004
PATENT & TRADEMARK OFFICE

Fig. 8



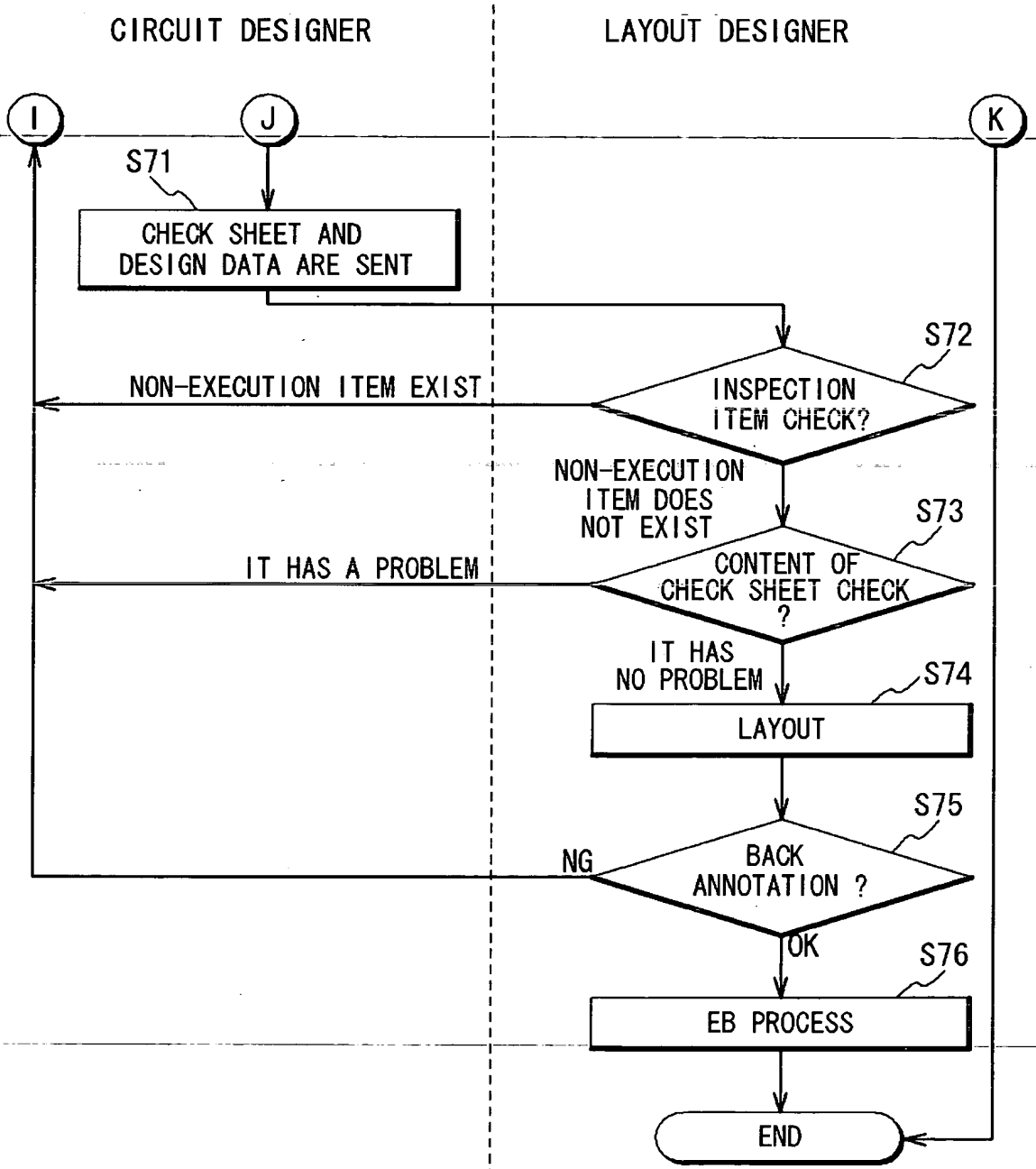
OIPE JC194
JAN 0 2 2004
PATENT & TRADEMARK OFFICE

Fig. 9



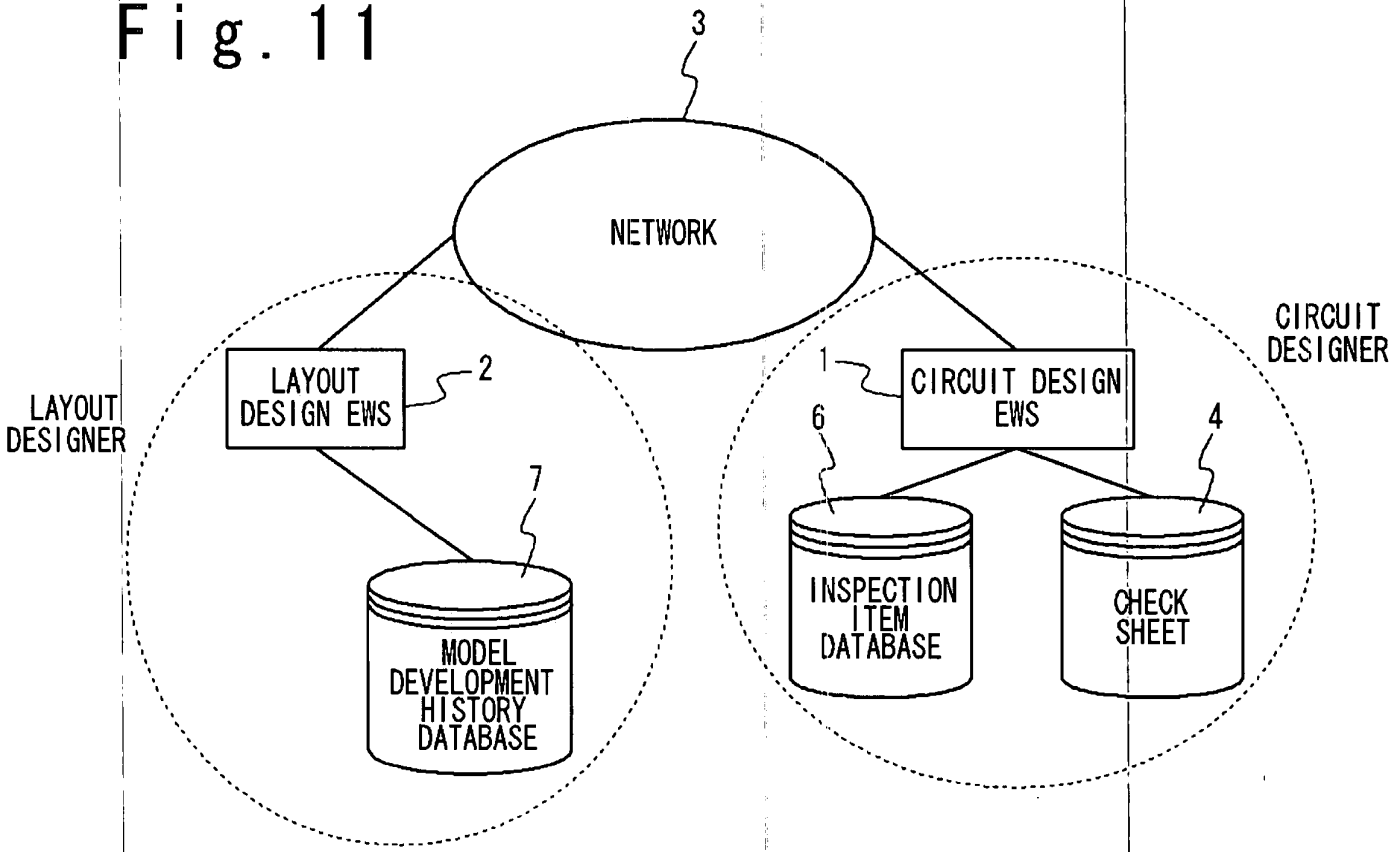
OIPE JC194
JAN 0 2 2004
PATENT & TRADEMARK OFFICE

Fig. 10



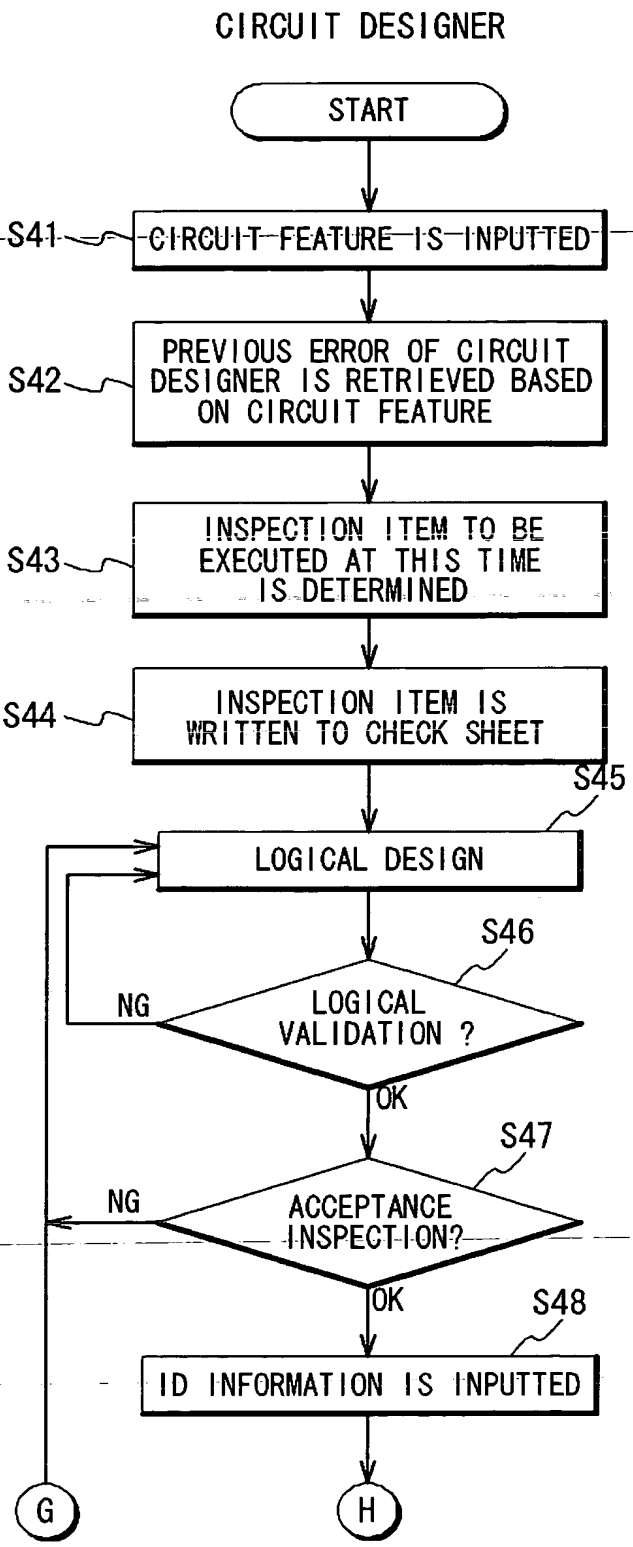
OIPE
JAN 0 2 2004
PATENT & TRADEMARK OFFICE
3C13

Fig. 11



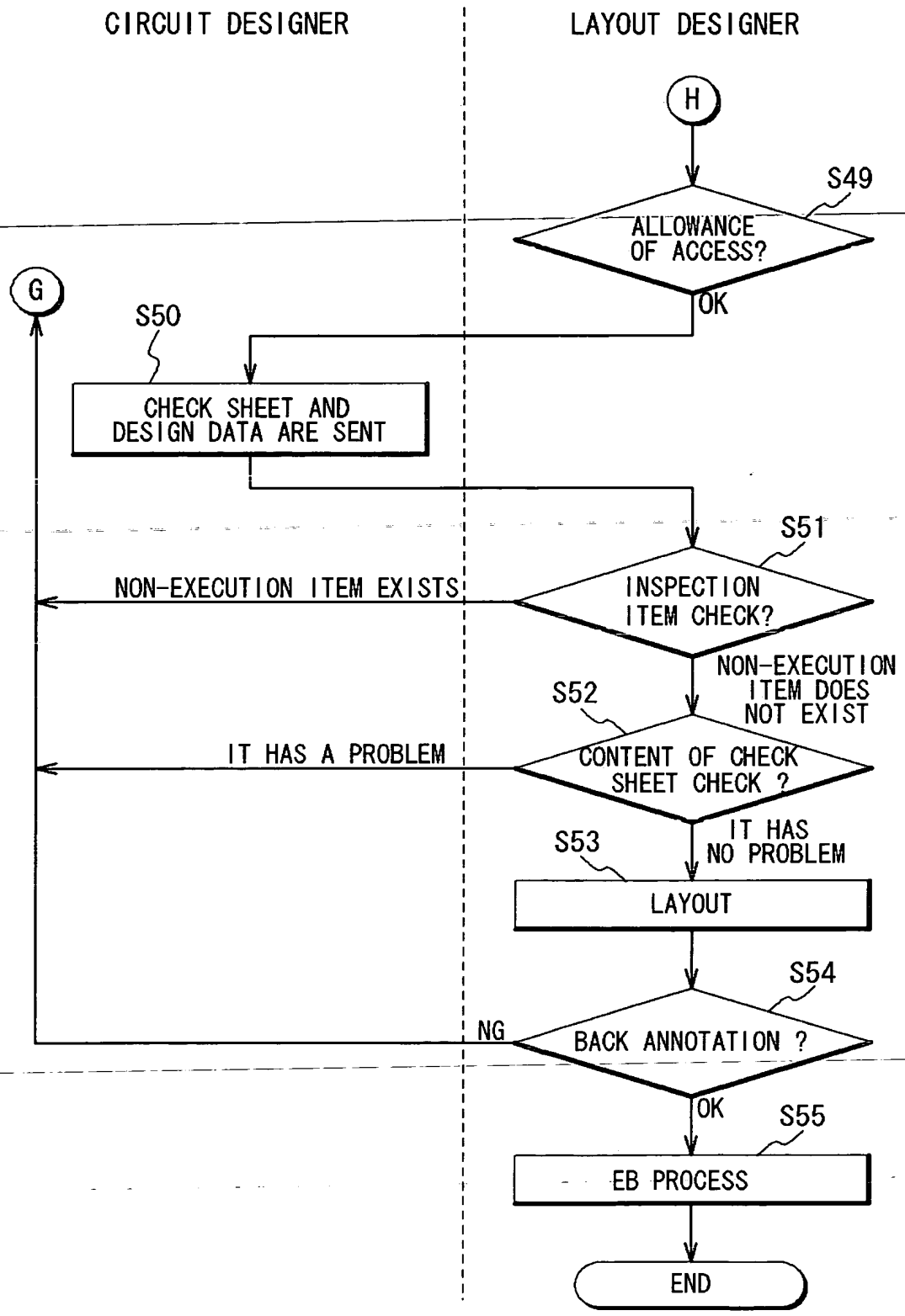
OIPE JC194
JAN 0 2 2004
PATENT & TRADEMARK OFFICE

Fig. 12



OIPE JC164
JAN 0 2 2004
PATENT & TRADEMARK OFFICE

Fig. 13



OIPE
JAN 0 2 2004
PATENT & TRADEMARK OFFICE
JC194

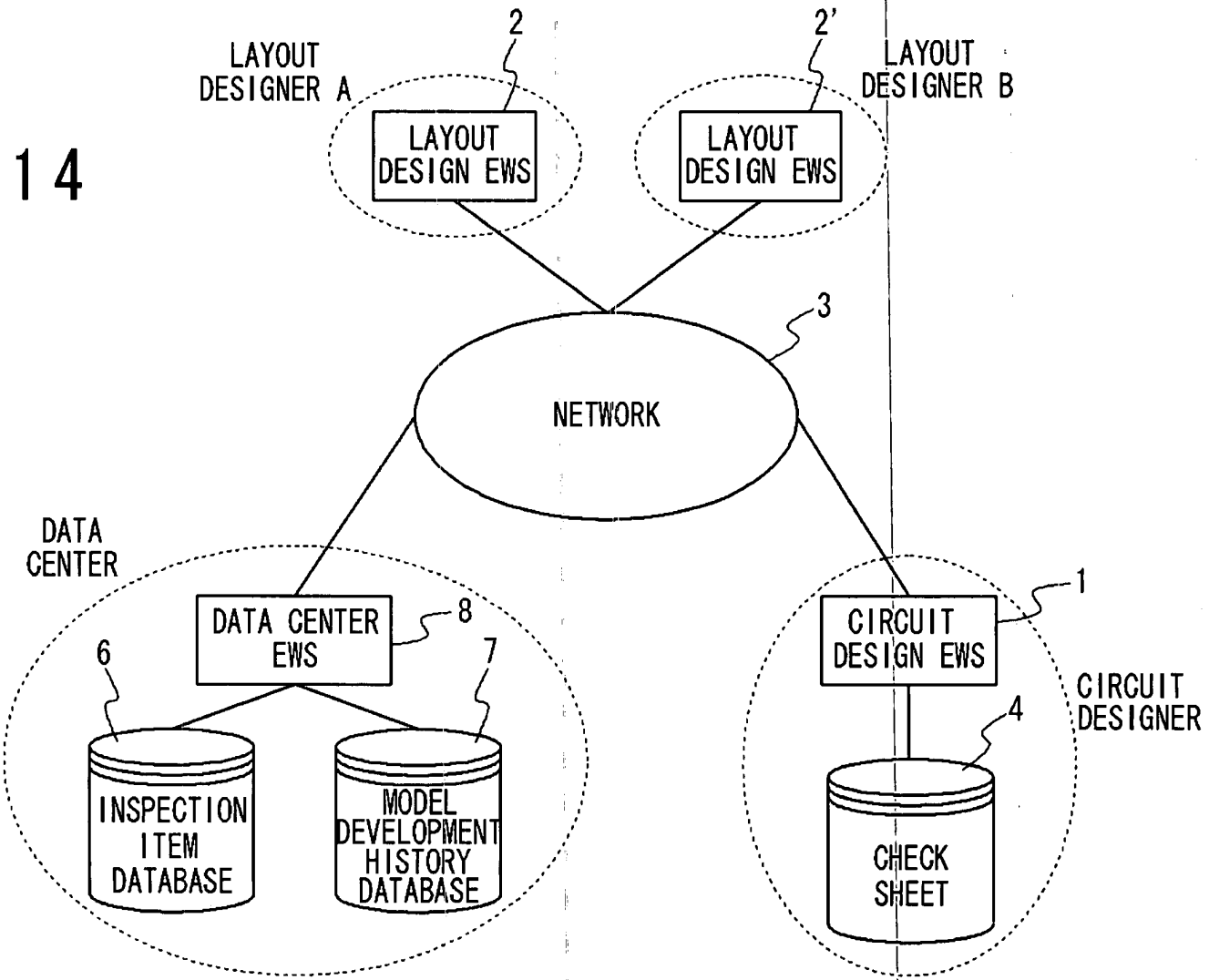



Fig. 14